IN THE SPECIFICATION:

Please delete the paragraphs on page 1, line 2 and page 1, line 3 of the specification.

Please add the following new paragraph before page 1, line 4 of the specification.

FIELD OF THE INVENTION

Please add the following new paragraph before page 1, line 6 of the specification.

BACKGROUND OF THE INVENTION

Please replace the paragraph beginning at page 1, line 14 of the specification with the following amended paragraph.

A switching power supply of the ~~traditional~~ conventional type comprises a DC-DC converter and an input stage connected with the electric network and constituted by a full wave rectifier diode bridge and by a capacitor connected immediately downstream for producing a ~~not-regulated~~ non-regulated continuous voltage that ~~derives~~ is derived from the alternated sinusoidal network voltage. The capacitor has a ~~capacity~~ capacitance great enough that a relative low undulation with respect to the ~~continuos~~ continuous level is present at its terminals. The rectifier diodes of the bridge also will conduct only for a small portion of each half cycle of the network voltage because the instantaneous value thereof is lower than the voltage at the terminals of the capacitor for the greatest part of the cycle. Consequently the current ~~adsorbed~~ absorbed from the network will be constituted by a series of narrow pulses the amplitude of which is 5-10 times the resulting average value.

Please replace the paragraph beginning at page 1, line 27 of the specification with the following amended paragraph.

This presents considerable consequences: the current ~~adsorbed~~ absorbed from the network has peak values and ~~efficacious~~ effective values which are much higher than those in the case of ~~adsorbing~~ absorbing sinusoidal current, the network voltage is distorted due to the almost simultaneous pulse ~~adsorption~~ absorption of all the users connected with the network, in the case

of three-phase systems the current in the neutral conductor is increased and a low use of the power potentialities of the electric power systems occurs. In fact, the pulse current waveform has many odd harmonics which, even if they do not contribute to the power supplied to the load, contribute to increase the ~~efficacious~~ effective current ~~adsorbed~~ absorbed from the network and also to increase the power dissipation.

Please replace the paragraph beginning at page 2, line 7 of the specification with the following amended paragraph.

Quantitatively this can be expressed both as Power Factor (PF), that is the ratio between the real power (that supplied to the load by the power supply which is added to the power dissipated internally as heat)[[,]] and the apparent power (the product of the network ~~efficacious~~ effective power by the absorbed ~~efficacious~~ effective power), and as Total Harmonic Distortion (THD), which usually is the percent ratio between the energy associated ~~to~~ with all the superior level harmonics and that associated ~~to~~ with the main harmonic. Usually a power supply provided with a capacitive filter has a PF comprised between 0.4 and 0.6 and a THD higher than 100%.

Please replace the paragraph beginning at page 2, line 16 of the specification with the following amended paragraph.

A PFC, placed between the rectifier bridge and the input of the DC-DC converter, allows there to ~~adsorb~~ be absorbed from the network a current which is almost sinusoidal and in phase with the voltage, by making the PF near 1 and by reducing the THD.

Please replace the paragraph beginning at page 3, line 8 of the specification with the following amended paragraph.

The control device 1 must keep the output voltage Vout at a constant value by means of a feedback control action. The control device 1 comprises an error operational amplifier 3 adapted to compare a part of the output voltage Vout, which is the voltage Vr given by Vr=R2*Vout/(R2+R1) (wherein the resistors R1 and R2 are connected in series with each other and are connected in parallel with the capacitor Co) with a voltage reference Vref, for example of

the value of 2.5V, and it generates an error signal proportional to the difference thereof. The output voltage Vout presents an undulation at a frequency that is twice the network frequency and which is superimposed ~~to~~ on the continuous value. However if the bandwidth of the error amplifier is ~~considerable~~ considerably reduced (typically it is lower than 20 Hz) by means of a suitable compensation network comprising at least one capacitor and if ~~an~~ operation in an almost stationary regime is assumed, that is if the input ~~efficacious~~ effective voltage and the load are constant, such undulation will be ~~considerable~~ considerably reduced and the error signal will become constant.

Please replace the paragraph beginning at page 3, line 23 of the specification with the following amended paragraph.

The error signal Se is sent to a multiplier 4 wherein it is multiplied by a signal Vi that is a part of the network voltage rectified by the diode bridge 2. At the output of the multiplier 4 a signal Sm will occur which is given by a rectified sinusoid, the width ~~thereof~~ of which will depend certainly on the network ~~efficacious~~ effective voltage and on the error signal Se.

Please replace the paragraph beginning at page 3, line 28 of the specification with the following amended paragraph.

The signal Sm is sent to the non-inverting input of a PWM comparator 5 while at the inverting input the signal Srs is applied, which signal occurs on the resistance Rs. If the signals Srs and Sm are equal the comparator 5 sends a signal to the control block 6 that is adapted to drive the transistor M and which, in this case, ~~provides to turn~~ turns it off ~~it~~. In such a way the output signal Sm of the multiplier determines the peak current of the transistor M and it will be enveloped by a rectified sinusoid. A filter placed at the input of the stage eliminates the component at the commutation frequency and provides the current ~~adsorbed~~ absorbed from the network ~~to have~~ the shape of the sinusoidal envelope. The block 6 comprises a block 7 adapted to detect the current zeros and able to send a pulse signal to an OR gate 8, the other input terminal of which is connected with a starter 10, which is adapted to send a signal to the OR gate 8 at the start time instant; the output signal S of the OR gate 8 is the set input of the set-reset flip-flop 11

~~having~~ which has another input R that is the output signal of the device 5, and which has an output signal Q. The signal Q is sent ~~at~~ to the input of a driver 12 which controls the turning on and off of the transistor M.

Please add the following new paragraph before page 6, line 3 of the specification.

SUMMARY OF THE INVENTION

Please add the following new paragraph before page 7, line 5 of the specification.

BRIEF DESCRIPTION OF THE DRAWINGS

Please add the following new paragraph before page 7, line 18 of the specification.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Please replace the paragraph beginning at page 8, line 7 of the specification with the following amended paragraph.

The PFC comprises a control circuit 100 able to keep the output voltage Vout at a constant value by means of a feedback control action. The control device 1 comprises an error amplifier 3 adapted to compare a part of the output voltage Vout, which is the voltage Vr given by Vr=R2*Vout/(R2+R1) (wherein the resistors R1 and R2 are connected in series with each other and are connected in parallel with the capacitor Co) with a voltage reference Vref, for example of the value of 2.5V, and it generates an error signal Se proportional to the difference thereof. The output voltage Vout presents an undulation at a frequency that is twice the network frequency and which is superimposed ~~to~~ on the direct value. However if the bandwidth of the error amplifier is ~~considerable~~ considerably reduced (typically it is lower than 20 Hz) by means of a suitable compensation network comprising at least one capacitor and if ~~an~~ operation in an almost stationary regime is assumed, that is if the input ~~efficacious~~ effective voltage and a load ~~which~~ are constant, such undulation will be ~~considerable~~ considerably reduced and the error signal will become constant.

Please replace the paragraph beginning at page 8, line 23 of the specification with the following amended paragraph.

The error signal Se is sent to a multiplier 4 wherein it is multiplied by a signal Vi that is a part of the network voltage rectified by the diode bridge 2. At the output of the multiplier 4 a signal Sm will occur which is given by a rectified sinusoid, the width ~~thereof~~ of which will depend certainly on the network ~~efficacious~~ effective voltage and on the error signal Se.

Please replace the paragraph beginning at page 9, line 10 of the specification with the following amended paragraph.

In such a way the output signal Sm of the multiplier determines the peak current of the transistor M and it will be enveloped by a rectified sinusoid. A filter placed at the input of the stage eliminates the component at the commutation frequency and provides the current ~~adsorbed~~ absorbed from the network ~~to have~~ the shape of the sinusoidal envelope.

Please replace the paragraph beginning at page 9, line 15 of the specification with the following amended paragraph.

The control circuit 100 comprises also a comparator 101 having the voltage signal Vr at the inverting input terminal and a voltage reference Vth at the non-inverting terminal. The output of the comparator is connected with one input of an AND gate 102, at the other input of which is present the output signal of a monostable multivibrator 103 controlled by the output signal of the PWM comparator 5. Alternatively the multivibrator 103 may be activated by a signal P, that is the ~~denied~~ negated signal Q, which is at the output of the flip-flop 11. The output of the AND gate 102 is connected with a set-reset flip-flop 104.

Please replace the paragraph beginning at page 9, line 24 of the specification with the following amended paragraph.

A switch SW is placed between the output terminal 31 of the error amplifier 3 and the terminal of the capacitor C which is coupled with the output of the error amplifier 3, and is controlled so as to interrupt the flow of the signal Se into the ~~analogic~~ analog multiplier for a

time period T when the comparator 5 sends the reset signal R to the flip-flop 11. The time period T is a small duration time period, for example 1ms, that occurs in each operation cycle of the control device 100, that is for each period Tciclo comprising the on time Ton of the MOS transistor M and the off time Toff of the same transistor M.

Please replace the paragraph beginning at page 10, line 13 of the specification with the following amended paragraph.

In Figure 4 a circuit scheme of a PFC for a switching power supply according to a variant of the first embodiment of the present invention is shown. The PFC comprises the converter 20 and a control circuit 200 that is similar to the control circuit 100 in Figure 3 except for comprising a holding sampling device 201 that is placed between the switch SW and the ~~analogic~~ analog multiplier 4 and which is driven by the output terminal of the PWM comparator 5. The device 201 memorizes the value of the output signal Se of the error amplifier 3 when the reset signal R is emitted. In such a way the disturbances that may be inducted in the multiplier 4 during its normal operation because of the opening of the switch SW are reduced.

Please replace the paragraph beginning at page 10, line 23 of the specification with the following amended paragraph.

In Figure 5 a circuit scheme of a PFC for a switching power supply according to a second embodiment of the present invention is shown. The PFC comprises a converter 20 and a control circuit 300 that is similar to the control circuit 100 in Figure 3 except for comprising a device 301 able to measure the current Se furnished by the error amplifier 3 and which is placed between the input of the multiplier 4 downstream of the switch SW and the compensation capacitor C. Said current Se is compared with a current reference inside the device 301 and, if the current Se is higher than the current reference, it sends to the output a signal S which, in combination with the reset signal R sent by the PWM comparator 5, determines the opening of the switch SW. ~~More in~~ In more detail the control circuit 300 comprises also a set-reset flip-flop 302, the set signal of which is the signal S of the device 301 and the reset signal is the output signal of the multivibrator 102; an AND gate 303, which has ~~having~~ in input the output signal Q

of the flip-flop 302 and the ~~denied~~ negated output signal of the multivibrator 103, controls the switch SW which therefore is no longer controlled directly by the output signal of the multivibrator 103. The flip-flop 302 allows ~~to avoid~~ oscillations of the switch to be avoided.

Please add the following new paragraph after page 11, line 19 of the specification.

What is claimed is: